

REMARKS

Claims 1-17, 19-42, and 45-50 are pending in the present application. Claims 18, 43, and 44 have been cancelled without prejudice or disclaimer to the subject matter contained therein.

A. Rejection of Claims 1, 2, 4-7, 18, and 35-37 as being anticipated by Kameyama et al.

Claims 1, 2, 4-7, 18, and 35-37 have been rejected under 35 U.S.C. §102(b) as being anticipated by Kameyama et al. (US-A-5,748,053). This rejection under 35 U.S.C. §102(b) to claims 1, 2, 4-7, 18, and 35-37, and as it also may be applied to newly added claims 47-50, is respectfully traversed.

As respectfully submitted above, amended independent claim 1 sets forth a switch comprising a plurality of field effect transistors connected in series, each field effect transistor including a gate, a source, and a drain, each gate having a gate width and a gate length. The gate length of one of the series connected field effect transistors is a different size from the gate length of another series connected field effect transistor.

Independent claim 18 has been cancelled without prejudice or disclaimer to the subject matter contained therein.

Moreover, amended independent claim 35 sets forth a radio frequency single pole double throw switch comprising a receiver port; a transmitter port; an antenna port; a receiver section connecting the receiver port to the antenna; and a transmitter section connecting the transmitter port to the antenna. The receiver section includes a first receiver dual-gate high electron mobility transistor having gates of different lengths and a second receiver dual-gate high electron mobility transistor having gates of different lengths.

Newly added independent claim 47 sets forth a series connected dual-gate transistor comprising a first gate and a second gate. The first gate has a gate width and a gate length, and the second gate has a gate width and a gate length. The gate length of the first gate is a different size from the gate length of the second gate.

Newly added independent claim 49 sets forth a dual-gate transistor having gates with different size lengths. Lastly, newly added independent claim 50 sets forth a dual-gate transistor having gates with different size lengths, the gates having different size widths.

In formulating the rejection under 35 U.S.C. §102(b), the Examiner alleges that Kameyama et al. teaches a switch having a plurality of field effect transistors (712-713) connected in series, each field effect transistor including a gate, a source, and a drain. The Examiner further alleges that Kameyama et al. teaches that the gate of one of the series connected field effect transistors is a different size from the gate of another series connected field effect transistor. This position by the Examiner is respectfully traversed.

Kameyama et al. only teaches that the gates' peripheries are of different sizes. A gate's periphery is the gate's width. In contrast, amended independent claim 1 states that the gate's length of one of the series connected field effect transistors is a different size from the gate's length of another series connected field effect transistor. The different size gate widths teaching of Kameyama et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 1.

With respect to amended independent claim 35, amended independent claim 35 states that the receiver section includes a first receiver dual-gate high electron mobility transistor having gates of different lengths and a second receiver dual-gate high electron mobility transistor having gates of different lengths. As noted above, Kameyama et al. only teaches that the gates' peripheries are of different sizes. The different size gate widths teaching of Kameyama et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 35.

With respect to newly added independent claim 47, independent claim 47 states that a series connected dual-gate transistor includes a first gate and a second gate wherein the gate length of the first gate is a different size from the gate length of the second gate. As noted above, Kameyama et al. only teaches that the gates' peripheries are of different sizes. The different size gate widths teaching of Kameyama et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 47.

With respect to newly added independent claim 49, independent claim 49 states that a dual-gate transistor has gates with different size lengths. As noted above, Kameyama et al. only teaches that the gates' peripheries are of different sizes. The different size gate widths teaching

of Kameyama et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 49.

Lastly, with respect to newly added independent claim 50, independent claim 50 states that a dual-gate transistor has gates with different size lengths, the gates having different size widths. As noted above, Kameyama et al. only teaches that the gates' peripheries are of different sizes. The different size gate widths teaching of Kameyama et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 50.

In summary, Kameyama et al. only teaches that the gates' peripheries are of different sizes. Therefore, since Kameyama et al. only teaches that the gates' peripheries are of different sizes, Kameyama et al. fails to anticipate different size gate lengths, as set forth by the various independent claims discussed above.

Accordingly, in view of the amendments and remarks set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection.

B. Rejection of Claims 1, 2, 4-6, and 18 as being anticipated by Tanaka et al.

Claims 1, 2, 4-6, and 18, have been rejected under 35 U.S.C. §102(b) as being anticipated by Tanaka et al. (EP- 0,700,161). This rejection under 35 U.S.C. §102(b) to claims 1, 2, 4-6, and 18, and as it also may be applied to newly added claims 47-50, is respectfully traversed.

As respectfully submitted above, amended independent claim 1 sets forth a switch comprising a plurality of field effect transistors connected in series, each field effect transistor including a gate, a source, and a drain, each gate having a gate width and a gate length. The gate length of one of the series connected field effect transistors is a different size from the gate length of another series connected field effect transistor.

Independent claim 18 has been cancelled without prejudice or disclaimer to the subject matter contained therein.

In formulating the rejection under 35 U.S.C. §102(b), the Examiner alleges that Tanaka et al. teaches a switch having a plurality of field effect transistors (**FET2-2, FET2-1, FET3**) connected in series. The Examiner further alleges that Tanaka et al. teaches that each field effect transistor includes a gate, a source, and a drain wherein the gate of one of the series connected

field effect transistors is a different size from the gate of another series connected field effect transistor. This position by the Examiner is respectfully traversed.

Tanaka et al. only teaches that the gates' peripheries are of different sizes. A gate's periphery is the gate's width. In contrast, amended independent claim 1 states that the gate's length of one of the series connected field effect transistors is a different size from the gate's length of another series connected field effect transistor. The different size gate widths teaching of Tanaka et al. fails to anticipate different size gate lengths, as set forth by amended independent claim 1.

In summary, Tanaka et al. only teaches that the gates' peripheries are of different sizes. Therefore, since Tanaka et al. only teaches that the gates' peripheries are of different sizes, Tanaka et al. fails to anticipate different size gate lengths, as set forth by the various independent claims discussed above.

Accordingly, in view of the amendments and remarks set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection.

CONCLUSION

Accordingly, in view of the amendments and remarks set forth above, the Examiner is respectfully requested to reconsider and withdraw all the present rejections. Also, an early indication of allowability is earnestly solicited.

Respectfully submitted,



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